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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/025,816	12/26/2001	Richard Slobodnik	550-299	4369
23117	7590	06/02/2005	EXAMINER	
NIXON & VANDERHYE, PC 901 NORTH GLEBE ROAD, 11TH FLOOR ARLINGTON, VA 22203				TABONE JR, JOHN J
ART UNIT		PAPER NUMBER		
		2133		

DATE MAILED: 06/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/025,816	SLOBODNIK ET AL.	
	Examiner John J. Tabone, Jr.	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 07 March 2005.
- 2a) This action is **FINAL**.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-34 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-34 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 02 April 2002 is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: \_\_\_\_\_.



**FINAL DETAILED ACTION**

1. Claims 1-34 remain in this application and have been examined. Claims 1, 7-10, 13, 18, 22-28, 30-32 and 34 have been amended.
2. Objections to the abstract and claims and rejection under 35 U.S.C. 112, second paragraph according to the previous office action of record are withdrawn by the Examiner as a result of Applicant's amendment.

***Response to Arguments***

3. Applicant's arguments filed 03/07/2005 have been fully considered but they are not persuasive.

As per arguments for independent claims 1 and 18:

The Applicant states "Lo neither discloses nor suggests that a self-test instruction is used to specify a test methodology to be applied by the self-test controller such that the self-test controller may be configured by the self-test instruction to implement different memory test methodologies". The Examiner asserts that Lo teaches that the ABIST engine 12 (self-test controller) receives a 9 bit word 13 from a Microcode Array 10 which stores a set of test program codes (self-test instruction) scanned-in (serially loaded) prior to ABIST test. Lo further discloses these 9 bits are divided into 5 fields: three bit Pointer field 14, one bit Address Increment field 15, three bit Data Control field 16, one bit Write Control field 17, and one bit End-Of-Address-Space control field 18.

(Col. 4, lines 31-37). Lo illustrates in Table 7 in Col. 10 that the value of the three bit Data Control field 16 (self-test instruction) specifies a test methodology to be applied to the memory array (i.e. WALKING, MARCHING, CHECKER\_BOARD, COLUMN\_STRIPE, etc.). In this the Examiner asserts that Lo teaches, "a self-test instruction is used to specify a test methodology to be applied by the self-test controller such that the self-test controller may be configured by the self-test instruction to implement different memory test methodologies."

In response to Applicant's argument on page 16, second paragraph to page 17, first paragraph that the reference fails to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., *The present invention provides the above-noted benefit in which the self-test instruction is used to specify a test methodology to configure the self-test controller, thereby providing additional flexibility without introducing a disadvantageous degree of complexity*) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

It is the Examiner's conclusion that independent claims 1 and 18 are not patentably distinct or non-obvious over the prior arts of record namely, Lo et al. (US-5661732). Therefore, the rejection is maintained. Based on their dependency on claims 1 and 18, claims 2-17 and 19-34, respectively, stand rejected.

***Claim Rejections - 35 USC § 102***

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-9, 13, 16, 17, 18-26, 30, 33 are rejected under 35 U.S.C. 102(b) as being anticipated by Lo et al. (US-5661732) hereafter Lo.

**Claims 1 and 18:**

Lo teaches a ABIST micro-processor block which consists of a Micro-code Array 10, the Registers 11a-11e, and the rest of the logic known as ABIST engine 12. Lo discloses that the ABIST engine 12 (self-test controller) receives a 9 bit word 13 from a Microcode Array 10 which stores a set of test program codes scanned-in prior to ABIST test (self-test controller configured by self-test instruction). Lo also teaches the ABIST (Array Built-In Self-Test) (self-test controller) is a small programmable micro-processor used to test and characterize on-chip arrays (at least one memory). (Col. 3, lines 61-63; col. 4, lines 28-33; FIG. 1). Lo teaches that the ABIST engine 12 (self-test controller) receives a 9 bit word 13 from a Microcode Array 10 which stores a set of test program codes (self-test instruction) scanned-in (serially loaded) prior to ABIST test. Lo further discloses these 9 bits are divided into 5 fields: three bit Pointer field 14, one bit Address Increment field 15, three bit Data Control field 16, one bit Write Control field 17, and one bit End-Of-Address-Space control field 18. (Col. 4, lines 31-37). Lo illustrates in Table 7 in Col. 10 that the value of the three bit Data Control field 16 (self-test instruction) specifies a test methodology to be applied to the memory array (i.e. WALKING, MARCHING, CHECKER\_BOARD, COLUMN\_STRIPE, etc.).

Claims 2 and 19:

Lo teaches that the ABIST engine 12 (self-test controller) receives a 9 bit word 13 from a Microcode Array 10 which stores a set of test program codes (plurality of self-test instructions) scanned-in prior to ABIST test. (Col. 4, lines 31-33). Lo further teaches the "sequences of memory tests" from the micro-programming examples starting in column 12, line 28 and ending column 16, line 11.

Claims 3 and 20:

Lo teaches the ABIST (Array Built-In Self-Test) 12 (self-test controller) is a small programmable micro-processor (processor) used to test and characterize (memory tests) on-chip arrays. Lo also teaches these arrays are adaptable (memory test can be changed) to state-of-the-art very/ultra large scale integration (VLSI or ULSI) chips which include the VLSI memory array elements 9 (different memories) which need to be self-tested. (Col. 3, lines 58-63).

Claims 4 and 21:

Lo teaches the programmable ABIST micro-processor block in Fig. 1 provides an improved method for testing and characterizing on-chip arrays in engineering, manufacturing, and burn-in environments (match fabrication characteristics) with programmable test patterns (different test needs), by implementing the testing of arrays with two different logical views. (Col. 3, lines 52-56).

Claims 5 and 22:

Lo teaches of a WALKING/MARCHING pattern in FIG. 5 which shows two loops. Lo further discloses that the minor or inner loop makes sure all words (rows) have done

their shift and the outer or major loop ensures that shifting has been done for all bit positions (columns). (Col. 10, lines 57-60).

Claims 6 and 23:

Lo teaches the Data Pattern Generation Logic 21 receives a 3 bit Data\_cntl code, ch\_abist\_data.sub\_ctrl(0:2), from the Micro-Code Array's field 16 to generate various data patterns for the Array-Under-Test (self-test instruction specifies data to be written to memory). (Col. 10, lines 10-13).

Claims 7 and 24:

**“...self-test controller allow one or more of the following memory test operations to be performed:**

**(iii) write specified data to memory locations having a checkerboard pattern of memory addresses;**

**(iv) read data from memory locations having a checkerboard pattern of memory addresses”**

Lo teaches of the reading and writing of a checkboard pattern with the following instructions: WO\_CHKB: Initialize the whole Array With ZEROs; Load dataReg with (0101...0101); Write inverted data as address advances to form CheckerBoard. Read CheckerBoard. Do the same with opposite data. (Col. 13, lines 7-10).

Claims 8 and 25:

Lo teaches the ABIST (Array Built-In Self-Test) 12 (self-test controller) is a small programmable micro-processor (processor) used to test and characterize on-chip arrays (on an integrated circuit). (Col. 3, lines 61-63).

Claims 9 and 26:

Lo teaches the memory arrays are adaptable to state-of-the-art very/ultra large scale integration (VLSI or ULSI) chips which include the VLSI memory array elements 9 (synthesized and custom memory) which need to be self-tested. (Col. 3, lines 58-60).

Claims 13 and 30:

Lo teaches data read out from the memory array also feed a bank of internal (within the array Macro) MISR registers (not shown) with feedback circuitry for signature generation (detect memory error). (Col. 4, lines 21-25).

Claims 16 and 33:

Lo teaches that the ABIST engine 12 (self-test controller) receives a 9 bit word 13 from a Microcode Array 10 which stores a set of test program codes (self-test instruction) scanned-in (serially loaded) prior to ABIST test. (Col. 4, lines 31-33).

Claims 17 and 34:

Lo teaches that the ABIST engine 12 (self-test controller) receives a 9 bit word 13 from a Microcode Array 10 which stores a set of test program codes (self-test instruction) scanned-in (external signal pin) prior to ABIST test. (Col. 4, lines 31-33).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

Art Unit: 2133

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 10, 11, 14, 27, 28 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al. (US-5661732) in view of Gold (US-2003/0167428 A1).

Claims 10 and 27:

Lo does not explicitly teach "interface circuit serving to adapted values and timings of signals passed between said self-test controller and said at least one memory to accommodate differing value and timing properties of said at least one memory." Gold teaches a memory address converter 24 (interface circuit) converts the physical address generated by the BIST engine 20 (self-test controller) to a corresponding logical address in the embedded memory 28 (memory). (Page 2, ¶ 17). Gold suggests the address converter 24 (interface circuit) may be adapted to support built-in self-repair of the embedded memory array 28 (at least one memory). (Page 2, ¶ 21). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lo's ABIST engine 12 (self-test controller) to couple Gold's address converter 24 (interface circuit) between Lo's next address calculation logic 20 and the memory array elements 9. Also, it would have been obvious to one of ordinary skill in the art at the time the invention was made that Gold's address converter 24 (interface circuit), in being adapted to support built-in self-repair of the embedded memory array 28 would contain the necessary circuitry to synchronize the timing of the signals connected to the memory array 28. The artisan would have been motivated to believe so because it would enable Lo's ABIST engine 12 (self-test controller) to accommodate differing value and timing properties of a memory. The artisan also, would have been motivated to

believe so because built-in self-repair circuits inherently adapt the repair circuit to the memory timing it is repairing through synchronization of the signals interfacing to the memory array. In this way the interface circuit of the instant application would already be included in Gold's address converter 24 (interface circuit).

Claims 11 and 28:

The motivation for combining Lo and Gold is per claims 10 and 27 rejection above. Gold teaches a memory address converter 24 (interface circuit) converts the physical address generated by the BIST engine 20 (address value generated by the self-test controller) to a corresponding logical address in the embedded memory 28 (memory). (Page 2, ¶ 17). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lo's ABIST engine 12 (self-test controller) to couple Gold's address converter 24 (interface circuit) between Lo's next address calculation logic 20 and the memory array elements 9. The artisan would have been motivated to do so because it would enable Lo's ABIST engine 12 (self-test controller) to access the logical addresses of the memory array elements 9.

Claims 14 and 31:

The motivation for combining Lo and Gold is per claims 10 and 27 rejection above. Lo does not explicitly teach of "a result data register included in the interface circuit". However, Lo does teach the data read out from the array also feed a bank of internal (within the array Macro) MISR registers (not shown) with feedback circuitry for signature generation. (Col. 4, lines 21-25). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lo's MISR registers

to be included in Gold's memory address converter 24 (interface circuit). The artisan would have been motivated to do so because it would enable Gold's memory address converter 24 (interface circuit), already incorporated in Lo's ABIST micro-processor block, to capture the test result data.

6. Claims 12, 15, 29 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al. (US-5661732), hereafter Lo, in view of Correale, Jr. et al. (US-6001662), hereafter Correale.

Claims 12 and 29:

Lo does not explicitly teach the "specifying which memory to test via the self-test instruction". However, Lo does teach "State Machine" 24 which determines how many passes the micro-program has to be repeated for different variations of operational parameters (self-test instruction) in testing the memory array elements 9 (plurality of memories). (Col. 4, lines 46-48). Correale teaches ABIST address counter 202 is coupled to a first memory array 205, a second memory array 206 and an "Nth" memory array 208 (plurality of memories). Correale also teaches that each memory array includes a generated address mask in order to access each memory array (specifying which memory to test via the self-test instruction). (FIG. 7, Col. 6, lines 29-61). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lo's state machine 24 to incorporate the address masking functions of Correale's ABIST address counter 202. The artisan would have been motivated to do so because this would enable Lo to specify which to plurality of memories test.

Claims 15 and 32:

Lo does not explicitly teach the "self-test instruction specifies a size of memory to be tested". However, Lo does teach "State Machine" 24 which determines how many passes the micro-program has to be repeated for different variations of operational parameters. (Col. 4, lines 46-48). Correale teaches an ABIST controller 92 is designed to work with a variety of different sized memory arrays (specifies a size of memory to be tested). Correale further teaches ABIST state machine 122 controls the number of iterations, the incrementing and decrementing of the addresses, when to examine array compare signals, and when to switch data patterns as well as read/write controls. Correale suggests no changes to ABIST state machine 122 are necessary to test multiple arrays of different sizes. (Col. 6 lines 10-15). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lo's state machine 24 with Correale's state machine 122. The artisan would have been motivated to do so because this would enable Lo to test memories of different sizes.

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

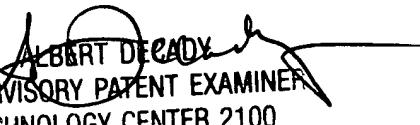
shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
John J. Tabone, Jr.  
Examiner  
Art Unit 2133

  
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